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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/943,667	08/31/2001	Shuichi Kikuchi	10417-094001	1120

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EXAMINER	
THOMAS, TONIAE M	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 11/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/943,667	KIKUCHI ET AL.	
	Examiner	Art Unit	
	Toniae M. Thomas	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3 and 8-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 8-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 19 August 2004 has been entered. Currently, claims 1-3 and 8-14 are pending.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 1-14 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claim 1 has been amended to recite the limitation *a first low concentration drain region of a second conductive type provided adjacent to one end of said gate electrode.* Similarly, claim 9 has been amended to recite the limitation *a*

first drain region provided adjacent to one end of said gate electrode in the semiconductor substrate. While the specification provides support for *a first low concentration drain region of a second conductive type at one end of the gate electrode*, and for *a first drain region provided at one end of said gate electrode*, the specification does not provide support for the claim language *a first drain region of a second conductive type adjacent to one end of said gate electrode*, as recited in amended claim 1 at lines 4-5, or for the claim language *a first drain region provided adjacent to one end of said gate electrode in the semiconductor substrate*, as recited in amended claim 9 at lines 5-6. As discussed in the letter mailed on 11 August 2004, in figure 4 of the originally filed drawings, source region 10 is self-aligned with the gate electrode 9. Figure 4 clearly shows the source region as being next to the gate electrode. Hence, the source region is adjacent to the gate electrode. This explicit definition of the term *adjacent to* is found in the specification at page 12, lines 7- 11. While the source region 10 is adjacent to the gate electrode 9, the first drain region 5 is not. Figure 4 clearly shows the gate region overlapping the first drain region. In other words, the first drain region is not self-aligned with the gate electrode. Since the gate electrode overlaps the first drain region, the term *adjacent to* does not accurately describe the structural relation of the first drain region to the gate electrode.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. *Claims 1, 8-11, and 14 are rejected under 35 U.S.C. 102(e) as being anticipated by Tung (US 6,117,738).*[1]

Regarding claims 1, 8-11, and 14

Tung discloses a semiconductor device (figs. 2A-2E and col. 3, lines 15 – col. 4, lines 22). The device comprises the following elements: a gate electrode 216 formed on a first conductive type semiconductor substrate 200 through a gate oxide film 214 (fig. 2D); a first low concentration drain region 206 of a second conductive type, provided adjacent to one end of the gate electrode (fig. 2D); a second low concentration drain region 210 of the second conductive type, provided in the first low concentration drain region (fig. 2D), the second low concentration drain region 210 being disposed close to an outer boundary of the first low concentration drain region 206 and being higher in impurity concentration than at least an impurity concentration of the first low

concentration drain region (col. 4, lines 4-7), wherein at least part of the second low concentration drain region is extended to an area under the gate electrode (2D); a high concentration source region 218 of the second conductive type provided adjacent to another end of the gate electrode, wherein the high concentration source region is in direct contact with the substrate (fig. 2D);[2] and a high concentration drain region 220 of the second conductive type formed in the second low concentration drain region, the high concentration drain region being spaced away a predetermined distance from the gate electrode and being higher in impurity concentration than the second low concentration drain region, as recited in claim 1 (fig. 2E and col. 4, lines 4-7).

Relatively, the first and second low concentration drain regions, 206 and 210, respectively, have low impurity concentrations, and the high concentration drain region 220 has a high impurity concentration, as recited in claim 8 (fig. 2E and col. 4, lines 4-7).

The second drain region 210 has a higher impurity concentration than the first drain region 206, and the third drain region 220 has a higher impurity concentration than the second drain region 210, as recited in claim 10 (col. 4, lines 4-7).

The first, second, and third drain regions 206, 210, and 220, respectively, and the source region 218 are of a second conductivity type, N-

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[1] The Tung reference was relied upon in the Office action mailed on 15 October 2003

type, and the semiconductor substrate 200 is of a first conductivity type, P-type, as recited in claim 11 (fig. 2E).

The first, second and third drain regions 206, 210, and 220, respectively, form a triple well structure in the semiconductor substrate such that the third drain region 220 is the innermost well, the second drain region 210 is the middle well surrounding the third drain region, and the first drain region 206 is the outermost well surrounding the second drain region, as recited in claim 14 (fig. 2E).

Regarding claim 9

Tung discloses a semiconductor device, the device comprising: a semiconductor substrate 200 (fig. 2A); a gate oxide film 202 provided on the semiconductor substrate (fig. 2A); a gate electrode 216 disposed on the gate oxide film (fig. 2D); a first drain region 206 provided adjacent to one end of the gate electrode in the semiconductor substrate (fig. 2D); a second drain region 210 provided in the first drain region 206, an outer boundary of the second drain region being disposed close to an outer boundary of the first drain region, wherein at least part of the second drain region is extended to an area under the gate electrode (fig. 2D); a third drain region 220 provided in the second drain region 210, the third drain region being spaced away a predetermined distance from the gate electrode and being spaced apart from the outer

[2] Since the high concentration source region 218 is implanted into the semiconductor material, which forms the semiconductor substrate 200, the region 218 is in direct contact with the substrate.

boundary of the second drain region (fig. 2E); and a region 218 of the second conductive type provided adjacent to another end of the gate electrode, wherein the region of the second conductive type is in direct contact with the substrate (fig. 2E), wherein the first, second, and third drain regions all having different impurity concentrations (col. 4, lines 4-7), as recited in claim 9.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. *Claims 2, 3, 12, and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tung in view of Wolf (Silicon Processing for the VLSI Era – Vol. 3: The Submicron MOSFET).*[3]

Tung lacks anticipation only in not teaching: that the first low concentration drain region 206 and the second low concentration drain region 210 are formed by utilizing two kinds of second conductive type impurities, wherein the two kinds of the second type conductive impurities have different diffusion coefficients, as recited in claims 2 and 12; and that the first drain region and the second drain region are formed using phosphorus and arsenic ions, respectively, as recited in claims 3 and 13.

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[3] The Wolf reference was relied upon in the Office action mailed on 15 October 2003.

Wolf discloses a double diffused drain (DDD) structure for an NMOS field effect transistor (pages 588-590). The DDD structure comprises a first drain region n^- and a second drain region n^+, wherein the first drain region has a lower concentration than the second drain region (fig. 9-26). The first drain region and the second drain region are formed using two kinds of N-type impurities, phosphorus and arsenic, which have different diffusion coefficients (page 588, third paragraph). The first drain region n^- is formed using phosphorus ions, and the second drain region is formed using arsenic ions.

The DDD structure in Wolf is formed by co-implanting phosphorus and arsenic ions into the same region using two separate implants, and performing a high temperature anneal. The anneal causes the phosphorus and arsenic ions to diffuse simultaneously resulting in the DDD structure. Because phosphorus diffuses faster than arsenic, the phosphorus ions are driven farther than the arsenic ions. This creates a less abrupt concentration gradient for the drain region (page 588, third paragraph).

Since both Tung and Wolf disclose an NMOS transistor comprising a drain region, wherein the drain region has a concentration gradient, the purpose disclosed by Wolf would have been recognized in Tung by one of ordinary skill in the art at the time the inventions was made.

One having ordinary skill in the art would have been motivated to modify the NMOS transistor of Tung, at the time the invention was made, such that the first and second drain regions are formed by utilizing two kinds of second

conductive type impurities, the two kinds of the second type conductive impurities having different diffusion coefficients, and such that the first drain region and the second drain region are formed using phosphorus and arsenic ions, respectively, since phosphorus diffuses faster than arsenic and, thereby creates a less abrupt concentration gradient for the drain region.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Toniae M. Thomas whose telephone number is (571) 272-1846. The examiner can normally be reached on Monday-Thursday from 8:30 a.m. to 5:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JMJ
01 November 2004

Mary Wilczewski
Primary Examiner